DESIGN OF DUAL EDGE TRIGGERED SENSE AMPLIFIER FLIP-FLOP FOR LOW POWER APPLICATION

[1]KISHORI S. GHUKSE, [2]N. A. PANDE, [3]MINAL S. GHUTE

[1,2,3]Department of Electronics and Telecommunication, Yeshwantrao Chavan College of Engg., Nagpur, India.
E-mail: kishorighukse26@gmail.com, j_nive13dec@yahoo.co.in, minal_ghute@rediffmail.com

Abstract- Dual edge triggered sense amplifier flip-flop for low power application is presented in this paper. This system is implemented using advanced Electronic Design Automation (EDA) tools. Now a day as Complexity means transistor on chip increases the power requirement also get increases, so the power is an important in VLSI design. In VLSI circuit the major design issues are power consumption and speed. Power dissipation can be reducing by a compromise of variety of components. Power consumption is also data dependent in VLSI circuit (like in multipliers). This paper gives modular approach for optimizing power consumption. Low power design is not only used in small size devices but also in high performance computational devices. Flip-flop is important element to determine the power consumption in VLSI design level. In this paper dual edge triggered flip-flop's power consumption and optimization of delay is primarily figure of merit. To reduce power consumption, we have used explicit pulse generator and latch using precharching transistor in static output –controlled discharge flip-flop (SCDFF) and the conditional discharge technique is inserted. The dual-edge triggered static pulsed flip-flop (DSPFF) removes unnecessary transitions. Adaptive clocking dual-edge triggered sense amplifier flip-flop (ACSAFF) removes the redundant transition of internal nodes.

Keywords- Small Delay; Low-Power; Dual-Edge Triggered Flip-Flop; Static Output –Controlled Discharge Flip-Flop; Adaptive Clocking Dual-Edge Triggered Sense Amplifier Flip-Flop; Sense Amplifier

I. INTRODUCTION

Due to increasing number of transistors on a chip the complexity is increasing day by day. And as complexity increases the power dissipation also gets high. In synchronous VLSI circuit design the power dissipation is one of the very important constraints. In recent year the high speed required at low power consumption. Flip-Flops are the critical element in digital circuit design on high speed and low power consumption. The performance of Flip-Flop matters the most important at gate level design to increase the speed is required at low power consumption. The single edge triggered flip-flop requires more power as compared to the dual edge triggered flip-flop. Dual edge triggered flip-flop has half of the clock frequency at same throughput as in single edge triggered flip-flop. To design low power and low voltage VLSI circuit the dual edge triggered flip-flop gained more attention at gate level. As the transistor densities on chip increases then it requires more power dissipation and also speed of the devices also get decreases. Now days the high speed digital systems at low power dissipation is in great demand. In the design constraints the synchronous VLSI can be divided in three major factors as Power consumption in the clock network, in the clock buffer and in the flip-flop.

Flip-Flop is one of the most power consumption components. It accounts a 30% to 60% of total power of the system. In single edge triggered flip-flop the output follows the input at the one of the edge of the clock pulse. As compared in dual edge triggered flip-flop output follows the input on the both of the edge of the clock pulse. On the rising edge of clock pulse and falling edge of the clock pulse, the output is the given value of input otherwise the output can be unaffected. Since dual edge triggered flip-flop helps to reduced the clock frequency to the half that of the single edge triggered flip-flop at the same data throughput. Dual edge triggered flip-flop (DETFF) gain has advantage over single edged triggered flip-flop. It requires half of the frequency as in single edged triggered flip-flop. Dual edge triggered flip-flop (DETFF) reduce clock frequency at half of the single edged triggered flip-flop (SETFF) with same data throughput therefore it gives better performance in terms of power. Flip-flop is important element to determine the power consumption in VLSI design level.

II. LOW POWER DESIGN

In digital circuit the power dissipation is due to four sources such as switching power, short circuit power, leakage power and static power. To switch the circuit 90% of total power required and is also depend on the number of transistors and clock frequency. In the Flip-Flop Design required Small Clk-Output delay, Narrow sampling window, Low power, Small clock load, High driving capability. Typical flip-flop load in a 0.18µm CMOS ranges from 50fF to over 200fF, with typical values of 100-150fF in critical paths. Total power consumed by flip-flop is measured as internal power, data power, and clock power.

Power dissipation in CMOS is of two types: static dissipation and dynamic dissipation. Static dissipation of power is included Sub-threshold, current Gate

Leakage, Reverse-biased diode Leakage, and Contention current. And dynamic dissipation of power is due to Capacitive Switching, Short circuit or Gate Leakage**.** The power is reduced if the clock frequency is reduced. Short circuit power is a type of dynamic power and is small as compared with the switching power and is driven from the direct short circuit path. The leakage power is determined by the fabricated technology. Power reduces in VLSI to increase battery life time, costs, reduce use of natural resources, and increase system reliability.

In pulse triggered flip-flops, one is implicit pulse triggered flip-flop in which for generating the clock pulse implicit pulse generator is used and other one is explicit pulse triggered flip-flop in which generation of the clock pulse by explicit pulse generator technique is employed. In implicit pulse generation, the clock pulse is inside the flip-flop therefore cannot be used by the neighbouring flip-flops in the entire circuit. In explicit pulse triggered flip-flop, the pulse is generated externally by the pulse generator. In this type of the flip-flop can have the pulse generator being shared by the neighboring flip-flop, a technique which is not utilized in the implicit pulse triggered flip-flop. The number of transistors is less in this case as compared to the internal pulse generator type flip-flop. In gate level design of circuit, different combination of logical gates may produce same circuit output but different value of power consumption.

III. SENSE AMPLIFIER BASED FLIP-FLOP

The sense amplifier based flip-flop (SAFF) is Cross-coupled NAND -Speed bottleneck. It is also called as the cross-coupled set-reset (SR) latch which is present at the output stage. The new flip-flop uses a new output stage latch topology that considerably reduces delay and improves driving capability. The sense amplifier based flip-flop (SAFF) provides ratio less design, reduced short-circuit power dissipation, and glitch-free operation. It is proposed by Nikolic et al. The SAFF has improved the performances by using a symmetric slave latch collected of two Inverters and two complex CMOS gates. With an increased number of transistors in the output stage, which is composed of 16 MOS devices is paid by the performance gain.

The sense-amplifier stage can be used as a latch whose sampling window closes as soon as the stage switches. This guarantees that the circuit is capable of switching independently on circuit sizing. In addition, the sense amplifier based flip-flop (SAFF) is characterized by a near-zero setup time, a reduced hold time, a low clock load and true single phase operation.

These characteristics that build the SAFFs are good candidates to substitute conventional transmission-gate flip-flops in standard cell create approaches.

The SAFF has some disadvantages. The first being the glitching on the output nodes, which is more marked for light load conditions. The second disadvantage is due to the use of cross-coupled inverter latches that requires a suitable device sizing for a correct operation and undergo from crow-bar current that increases the power dissipation. A drawback of the conventional NAND-based SAFF is the high clock-to-output delay due to the slow output latch stage. Two high-speed slave latches have been proposed in the literature to make the speed of the SAFF analogous to or higher than the speed of the HLFF and the SDFF. SAFF is essential to distinguish it from the master–slave (MS) latch arrangement consisting of two cascade latches. MS latch pair can potentially be transparent if enough margins between the two clocking phases are not guaranteed. The pulse-generating stage of this flip-flop is such that it senses the accurate and opposite differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs the leading clock edge. Any change of the data during the active clock interval will not change the output of the SA. The SR latch captures the transition also holds the state until the next positive edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one. Therefore, the entire structure acts as a flip-flop.

IV. REVIEW OF STATE -OF- THE DUAL EDGE TRIGGERED FLIP-FLOP

A. Dual Edge-Triggered Static-Pulse Flip-Flop

Fig. 1 shows the schematic diagram of the dual-edge triggered static pulsed flip-flop (DSPFF). The four inverters are used in its pulse generator to produce the inverted and delayed clock signals. Produced signal apply to the nMOS transistors. These signals with these two nMOS pass transistors generate a narrow sampling window at both the rising edge and falling edges of the clock pulse. Once the pulse signal is generated by pulse generator, then the both pass transistors, N1 and N4, of static latch are turned on to capture the inputs data so that either SB or RB will be discharged. A smaller delay can be produced since DB and urge directly fed to the nodes, SB and RB, respectively. The two pMOS transistors, P1 and P2, two weak nMOS transistors and N2 and N3 are together which successfully avoid the floating of nodes. These node will be SB and RB when the flip-flop is transparent, thereby providing a fully static operation. The explicit pulse generator is simple and proper for dual-edge triggering. The static feature of DSPFF eliminates unnecessary transitions by cautiously sizing of the transistors aspect ratios symmetrical output delays can be obtained. However, the flip-flop latency may be falling due to the large capacitive loads at the SB and RB nodes. On top of that, dual-edge triggered static pulsed flip-flop (DSPFF) suffers from high leakage current. This is

caused by a high-voltage drop across one from transistor N2 or N3, when they are in turned off mode.

Fig. 1. Dual edge-triggered static pulsed flip-flop (DSPFF)

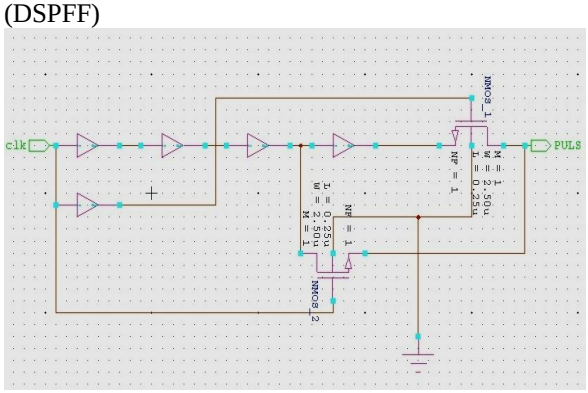

Fig. 1.(a) Dual pulse generator

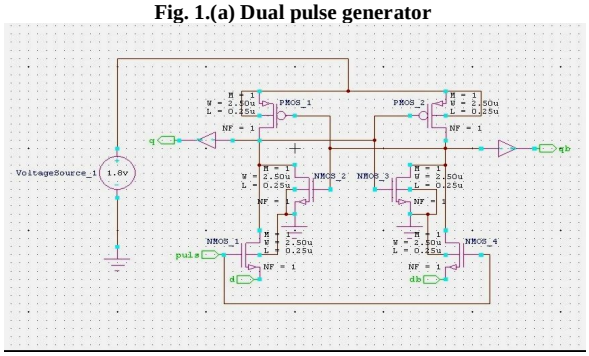

Fig. 1 (b) static latch

B. Static Output-Controlled Discharge Flip-Flop

Fig. 2 shows the schematic diagram of the static output-controlled discharge flip-flop (SCDFF). The static output-controlled discharge flip-flop (SCDFF) consists of two components such as pulse generator and latch. This involves an explicit pulse generator and a latch that captures the pulse signal which is generated by the pulse generator. The latch structure of SCDFF shown above consists of two static stages. The input signal presented as D. In the first stage, input signal D is used to drive the precharge transistor so that node X follows

D during the sampling period. In addition, the conditional discharging technique is used. This conditional discharge technique used to reduces the internal switching activities, and also generates a lesser amount of glitches at the output, while maintain the negative setup time and small delay characteristics. In the conditional capture technique results in redundant power consumed by the gate and controlling the delayed clock to the flip-flop. The conditional precharge technique has been applied only to implicit flip-flop represented as ip-FF, but it is complicated to use a double-edge triggering mechanism. A lot of transistor will required by these ipFF flip-flops. A new technique, conditional discharge technique, is proposed for both implicit and explicit pulse-triggered flip-flops without the problems associated with the conditional capture technique. In this technique, the extra switching activity is reduced by controlling the discharge path when the input is stable HIGH and thus the name Conditional discharge technique propose in. A QB-controlled nMOS is used to prevent unnecessary discharge by inserting this QB in the discharge path, which implemented conditional discharging technique. The conditional discharging technique is used to prevent unnecessary discharging at node X as long as the input remains high.

Fig. 2 Static output-controlled discharge flip-flop (SCDFF)

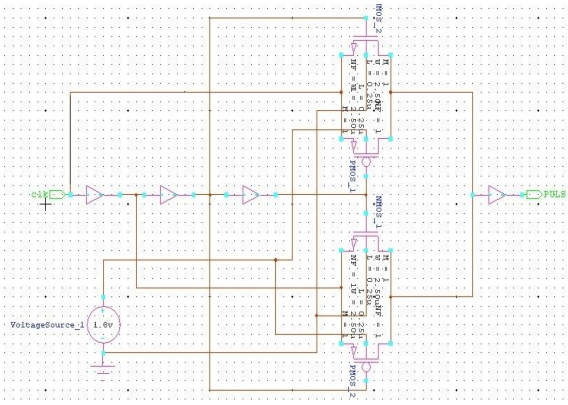

Fig. 2(a). dual pulse generator

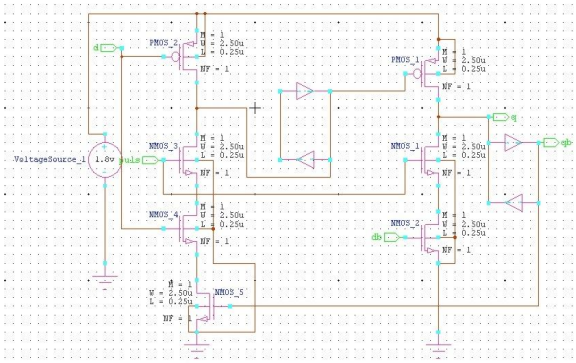

Fig. 2(b). Static latch.

C. Adaptive Clocking Dual Edge-Triggered Sense-Amplifier Flip-Flop

The schematic of adaptive clocking dual edge sense-amplifier flip-flop (ACSAFF) is shown in fig 3. Adaptive clocking dual edge sense-amplifier flip-flop (ACSAFF) consists of three components adaptive clocking inverter chain, front end sensing stage, and Nikolic's latch as shown in Fig. 3.

When the Q output is different from the D input, transistor N2 and N3 will turn ON, CLK will given to the inverter chain which produces the delayed clock signal. The transistor N2 and N3 be the transistor of inverter chain. Node SB and RB from frond end sensing stage forms a discharge path at falling and rising edges of the clock signal. As the output changes, transistor N4, N1, N3, N2 will stop to

charging. At the same time N8 and N5 or N6 and N7 will pull down the node to ground, and result of this transistor N2 and N3 are turn off and disable inverter chain. The adaptive clocking inverter chain used to disable some internal node through transistor when data switching activity is low.

The PMOS transistor P2 is used in inverter chain as control node whereas the CLK is low the output CLK4 will pull down to ground. Once CLK3 is pull to down, the transistor N3 turn off. This is done so that it is not influenced by input CLK signal. We pull down the CLK3 and CLK4 of inverter chain to preclude the front end sampling data without the rising and falling edge of CLK input. CLK3 and CLK4 will be high if this mechanism is not used.

Fig. 3. Adaptive clocking dual edge-triggered sense-amplifier flip-flop

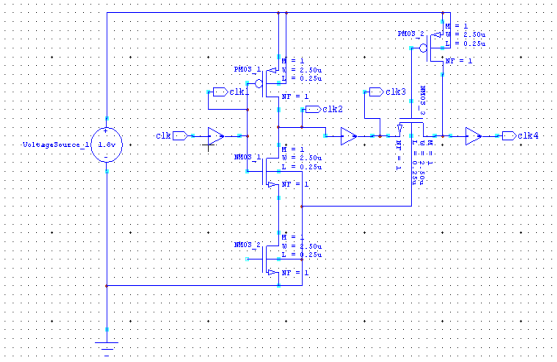

Fig. 3(a). Adaptive clocking inverter chain

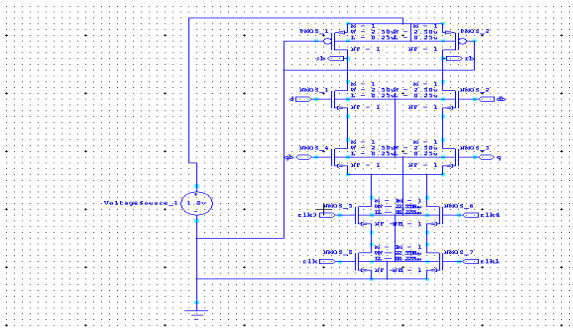

Fig. 3(b). Front end sensing stage

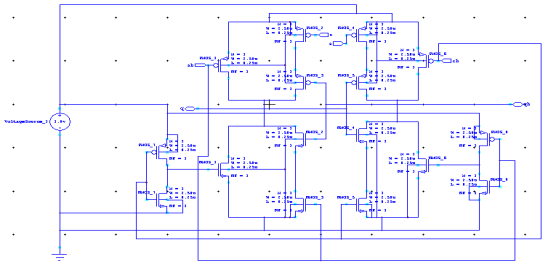

Fig. 3(c). Nikolic's latch.

V. SIMULATION RESULTS

The simulation results for all flip-flops are obtained in a 0.18µm CMOS technology at room temperature using T-SPICE that uses supply voltage is 1.8 V. Simulations of dual-edge triggered static pulsed flip-flop are shown in Fig.4. The average power of DSPFF is 1.0079µw.

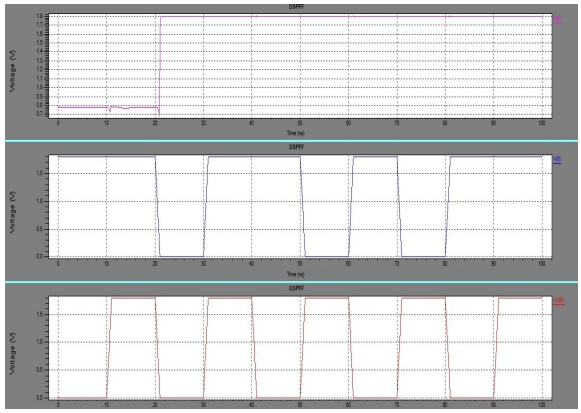

Fig. 4 Simulations of dual-edge triggered static pulsed flip-flop

Simulations of dual-edge triggered static pulsed flip-flop are shown in Fig.4 as D type flip-flop. That is the same as input data signal with a delayed signal. In this the clocking frequency is greater than input frequency, so input changes then it has delayed to observe at the output. The average power of DSPFF is 1.0079µw and by reducing threshold voltage power is reduced up to 0.757µw.

Simulations of dual-edge triggered static pulsed flip-flop are shown in Fig 5. And the conversional power of SCDFF is 0.1536µw. and using multithresolding technique it reduces up to 0.0357µw. From observation that power requirement is less than previous one.

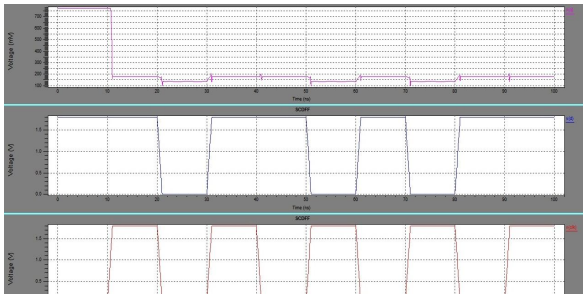

Fig. 5. Simulations of dual-edge triggered static pulsed flip-flop.

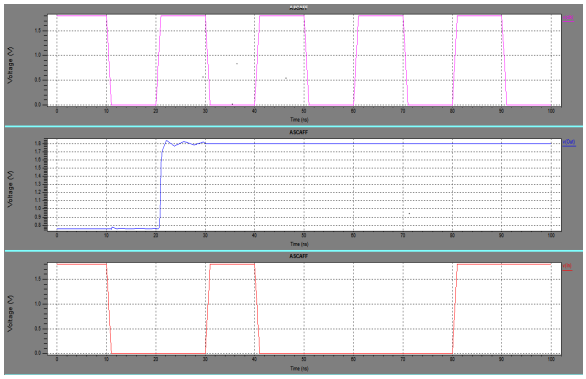

Fig. 6. Simulations of adaptive clocking dual edge sense-amplifier flip-flop (ACSAFF)

Power requirement to ACSAFF is 0.11472µw which is the conversional power required to ACSAFF. Using multithresolding technique it is reduced up to 0.050426µw.

CONCLUSION

In this paper, a new technique, conditional discharge, is introduced to reduce the switching activity of some internal nodes in flip-flops. This technique was utilized in a new flip-flop, dual-edge triggered static pulsed flip-flop Conditional discharge flip-flop, adaptive clocking sense amplifier flip-flop. Again to reduce power we used multi thresolding technique. And the comparison has done between conventional power and low power of flip-flop given below.

TABLE I

Name	Conventional power consumption	Power consumption reduced
SCDFF	0.1536µw	0.0357µw
DSPFF	1.0079µw	0.757µw
ACSAFF	0.11472µw	0.050426µw

REFERENCES

[1] Myintwaiphyu, Kangkangfu, Wang Ling Goh, Kiat –Seng Ye "Power –Efficient Explicit –Pulse Dual Edge Trigger Sense Amplifier Flip- Flop" IEEE transaction on VLSI system volum 19 Jan 2011.

[2] M. W. Phyu, W. L. Goh and K. S. Yeo "A Low-Power Static Dual Edge-Triggered Flip-Flop using an Output-Controlled Discharge Configuration" 0-7803-8834-8/05/$20.00 ©2005 IEEE.

[3] W. Chung, T. Lo, and M. Sachdev, "A comparative analysis of low power low-voltage dual-edge-triggered flip-flops," IEEE Transc. On Very Large Scale Integration (VLSI) Systems, vol. 10, pp. 913–918,Dec 2002.

[4] B.Nikolic,V.G.Oklobdzija,V.Stajanovic,W.Jia,J.K.Chiu,and M.M.Leung, "Improve Sense-Amplifier-Based Fip-Fop: Design and measurements," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876–883, Jun. 2000.

[5] Antonio G. M. Strollo, Davide De Caro, Ettore Napoli, and Nicola Petra "A Novel High-Speed Sense-Amplifier-Based Flip-Flop"IEEE Transactions on Very Large Scale Integration (VLSI) SYSTEMS, Vol. 13, No. 11, November 2005.

[6] P Zhao, T-K Darwish and M.A bayoumi "High – performance and low power condition discharge flip -flop" IEEE Tran on VLSI system May 2004.

[7] B. S. Kong, S. S. Kim, and Y. H. Jun, "Conditional-Capture flip-flop For Statistical Power Reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1263–1271, Aug. 2001.

[8] J. I. Kim and B. S. Kong, "Dual Edge-Triggered flip-flop With Modified NAND Keeper For High-Performance VLSI," Current Appl. Phys., Vol. 4, No. 1, pp. 49–53, Feb. 2004.

[9] G. Aliakbar and M. Hamid, "Dual-Edge Triggered Static Pulsed flip-flops," In Proc. 18th Int. Conf. VLSI Design 2005, Jan. 2005, pp. 846–849.

[10] C. K. The, M. Hamada, T. Fujita, H. Hara, N. Ikumi, And Y. Oowaki, "Conditional Data Mapping flip-flops For Low-Power And High-Perfor- Mance Systems," IEEE Trans. Very Large Scale Integral. (VLSI) Syst., vol. 14, no. 12, pp. 1379–1383, Dec. 2006.

[11] Yen-Ting Liu, Lih-Yih Chiou, Soon-Jyh Chang "Energy-Efficient Adaptive Clocking Dual Edge Sense-Amplifier Flip-Flop" 0-7803-9390-2/06/$20.00 ©) 2006 IEEE.

[12] Peiyi Zhao, Jason Mcneely,Pradeep Golconda,Magdy A. Bayoumi, Robert A. Barcenas, And Weidongkuang "Low-Power Clock Branch Sharing Double-Edge triggered Flip-Flop" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 15, NO. 3, MARCH 2007.

★★★