FIVE LEVEL DC-DC CONVERTER WITH ASYMMETRICAL CONTROL STRATEGY FOR HIGH POWER APPLICATIONS

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Abstract— In this paper an asymmetrical duty cycle control strategy was proposed to the TPTL dc/dc converter. The modified converter remains all the advantages of original control strategy; meanwhile, soft-switching can be achieved using the energy stored in output filter inductance and leakage inductances of transformers (or resonant inductances).Three-phase three-level (TPTL) dc/dc converter has the advantages of lower voltage and current stress on switches, which is suitable for high power and high input voltage applications. Adopting a symmetrical control strategy, the ripple frequency of input and output current can be increased significantly, resulting in a reduced filter requirement. To further reduce the current stress on switches for higher power. The improved resonant converter features zero-voltage-switching (ZVS) realization under wide load range and higher conversion efficiency. However, wide variation in switching frequency should be concerned in the applications with wide input/output voltage range. Other alternative solutions are the non resonant soft-switching three-phase converters, the upper and lower commutation cell switches are subjected to different current stresses is improved by using MAT Lab/Simulink. The proposed concept can be implemented with five level topology using Matlab/simulink software.

Keywords— Asymmetrical, Current Stress, Switching frequency, TPTL, ZVS.

I. INTRODUCTION

Over the years single phase full-bridge (FB) and three-phase FB pulsewidth modulation (PWM) dc to dc soft switched converters have become popular in the field of dc to dc conversion system. For these converters metal oxide semiconductor field effect transistors (MOSFETs) are generally preferred over insulated gate bipolar transistors (IGBTs), because they can be operated at higher switching frequency and they do not have the problem of long tail current. However, these FB PWM soft switched converters are not suitable for switch mode power supply applications, where the input voltage is high. This is because the MOSFETs have to sustain high input dc link voltage. Moreover, service of auxiliary circuits is required to operate devices in soft switched mode. This requires extra components, devices and hence it leads to incurring additional cost while reducing the system reliability. In order to reduce the voltage stress to half of the input dc voltage, a three-level topology has been considered in [1] and [2] for inverter application and it has been used for realizing a dc to dc converter in [3]–[5]. The soft commutation is achieved by using phase shift PWM modulation [4], [5] which is having simple control structure and high power density can be achieved. However at high power levels, these components experience considerable current stress. In order to overcome this problem, topologies consisting of three-phase inverter coupled to a three-phase high frequency transformer followed by three-phase high frequency bridge-rectifier have been proposed [6]–[9]. This results in an increase in the input current and output current frequencies by a factor of three as compared to the full bridge converter. This also results in lower current rating for the components and also a considerable reduction in size for the isolation transformer.

However, the devices experience high voltage stress and the control structure is also quite involved. In an effort to overcome the aforementioned limitations a new converter topology involving three-phase, three-level, (TPTL) phase shifted PWM converter involving six switches operating as zero voltage switching (ZVS) and six switches operating as zero current switching (ZCS) has been presented in this paper. It should be mentioned that in this case soft switching of the semiconductor devices is achieved without taking help from any additional auxiliary circuitry comprising of active or passive elements. In the proposed topology the output rectifier is a center tapped full wave current tripler [10], [11] producing either two or three-level output voltage depending on the operating duty cycle. This leads to considerable reduction in size of the output filter compared to that of the conventional full bridge topology.

II. MODIFIEDTPTL CONVERTER AND ASYMMETRICAL DUTY CYCLE CONTROL

Fig.1 shows the circuit configuration of TPTL converter in which, a three-phase transformer with –Y connection is employed for the smaller turns ratios and transformer VA rating. As shown, L_{ra}, L_{rb} and L_r care the additional resonant inductances to widen the ZVS commutation load range. L_{lka} ,L_{lkb}, and L_{lkc} are

the equivalent primary leakage inductances of each phase.

Df1 andDf2 are freewheeling diodes. C_{ss} is the flying capacitor, which is in favor of decoupling the switching transition ofQ_1,Q_3,Q_4, andQ_6. DR1−DR6 are rectifier diodes. The output filter is composed of Lf and C_f, and R_{Ld} is the load.

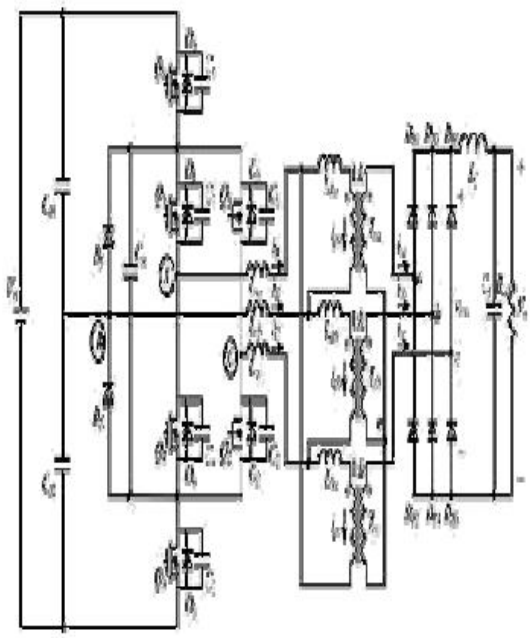

Fig.1. Topology configuration of TPTL dc/dc converter.

Fig.2 shows the switching sequences of the original control strategy and the modified control strategy, as shown in Fig. 2(a), Q1−Q6 are switched on in turn with interval of one-sixth switching period, the duty cycles of all switches are equal, and each switch has a maximum conduction period of 120◦. The required range for the duty cycle of any switch is from 0.167 to 0.33. Obviously, the two interleaved switches have a simultaneous turn-off interval, during which, the intrinsic capacitors of two switches will resonate with the leakage inductances of transformers for several periods. As the duty cycle of the switches varies with the input voltage and the load, the incoming switch cannot be ensured to turn on exactly when its drain-to-source voltage resonates to zero within the operation range; therefore, the switches suffer hard-switching and a considerable switching loss occurs. To realize the soft-switching for switches, the original interleaved switches should be designed in a complementary manner, and a short delay time t_d is necessary to be introduced between the two complementary switches to provide an interval for the ZVS commutation, which is similar to the control strategy of asymmetrical half-bridge converter. Accordingly, the duty cycles ofQ1,Q3, andQ5are served to regulate the output voltage, while the drive signals ofQ4,Q6, and Q2 are complementary to that of theQ1,Q3, and Q5, respectively. The obtained control strategy is illustrated in Fig. 2(b).

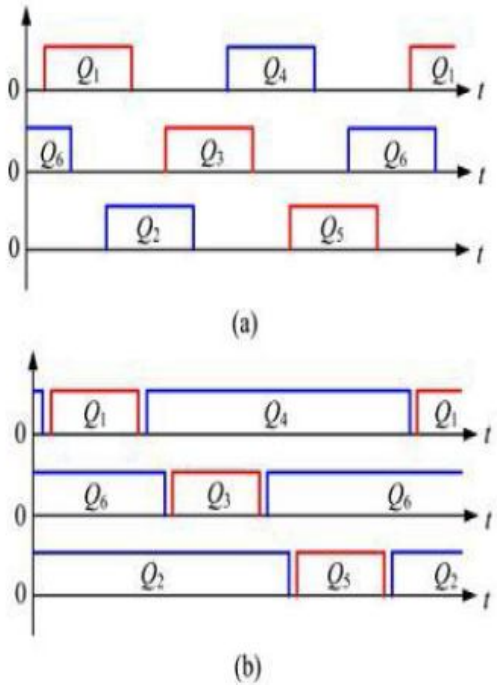

Fig. 2. Two kinds of control strategies of TPTL converter. (a) Symmetrical duty cycle control. (b) Asymmetrical duty cycle control.

III. OPERATION PRINCIPLE

This section will analyze the operation principles of the TPTL converter under the modified control scheme. The following assumptions are made for the simplicity before the analysis:

1) all power devices and diodes are ideal;
2) all capacitors and inductances are ideal;
3) the output filter inductance is large enough to be treated as a constant current source during a switching period; its value equals to output current Io;
4) the inductances of each phase are identical, i.e., L_{lka} =L_{lkb} =L_{lkc} =L_{lk},L_{ra}=L_{rb}=L_{rc}=L_r;
5) C_1 =C_2 =C_3 =C_4 =C_5 =C_6 =C_p.

Fig. 3 shows the key waveforms of the TPTL converter with asymmetrical duty cycle control, as seen, the operation of the TPTL converter can be classified by different modes, according to the duty cycle range and the load current. The corresponding operation modes are defined as the small duty cycle mode (SDCM), the medium duty cycle mode (MDCM), and the large duty cycle mode (LDCM), respectively, when the duty cycle varies between (0, 1/3), (1/3,Dr), and(Dr, 1/2), where Dr is a critical duty cycle that depends on the load current and the parameters of converter. The related waveforms in different operation modes are referred to Fig. 3(a)–(c). For simplicity, only the operation principle under SDCM will be described in this paper. As shown in Fig. 3(a), the converter has 18 operation stages during a switching period.

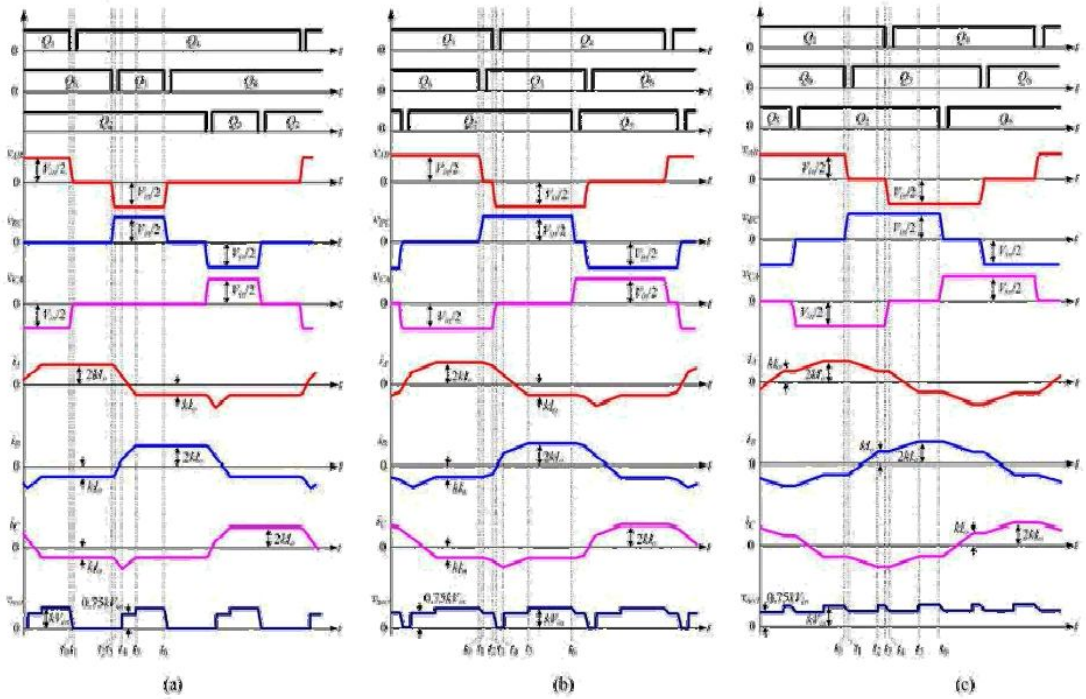

Fig.3. Key waveforms of the TPTL converter with asymmetrical duty cycle control. (a) SDCM. (b) MDCM. (c) LDCM

Fig. 4 shows seven operation stages of the converter under rated conditions. The other operation stages during the rest of a switching period are not depicted but they are symmetrically equivalent, expect for the fact that they are phase shifted.

The basic equations of the voltages and currents of the transformer are listed as follows:

$$v_{AB} + v_{BC} + v_{CA} = 0 \tag{1}$$

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2}$$

$$\frac{di_{pa}}{dt} = k\frac{di_{sa}}{dt} = \frac{v_{Llka}}{L_{lk}},\ \frac{di_{pb}}{dt} = k\frac{di_{sb}}{dt} = \frac{v_{Llkb}}{L_{lk}},\ \frac{di_{pc}}{dt} = k\frac{di_{sc}}{dt} = \frac{v_{Llkc}}{L_{lk}} \tag{3}$$

Where k represents the secondary-to-primary turns ratios of the transformer. The voltage across the leakage inductance of transformer can be derived from (2) and

(3) and is given as follows:

$$v_{Llka} + v_{Llkb} + v_{Llkc} = 0. \tag{4}$$

Stage1 [prior to t_0] [see Fig. 3.4(a)]: Prior to t0, Q_1, Q_2, Q_6, and $D_{f2}$are conducting at the primary side, andDR1andDR6 are conducting at the secondary side. v_{AB}=Vin/2, v_{BC}=0, and v_{CA}=−Vin/2. From (1), (2), (4), and other constraints between voltages and currents of transformers, the following expressions can be obtained:

Stage 2 [t_0,t_1] [see Fig. 4(b)]:At t_0,Q_1 is turned off, the line current $i_A$chargesC_1 and dischargesC_4 linearly, and the rectified voltage decreases. As C_1 limits the rising rate of the voltage acrossQ_1, Q_1 is zero-voltage turn-off. The voltages across$C_1$and C_4 are

$$v_{pa} = \frac{V_{\text{in}}}{2}, \qquad v_{pb} = 0, \qquad v_{pc} = -\frac{V_{\text{in}}}{2} \tag{5}$$

$$v_{\text{rect}} = v_{sa} - v_{sc} = k \cdot V_{\text{in}} \tag{6}$$

Where v_{pi} and v_{si} are the primary voltage and secondary voltage of transformers, I represents the subscripts a, b, and c.

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$$v_{C1}(t) = \frac{1}{C_p} \cdot k \cdot I_o \cdot (t - t_0) \tag{7}$$

$$v_{C4}(t) = \frac{V_{\text{in}}}{2} - \frac{1}{C_p} \cdot k \cdot I_o \cdot (t - t_0) \tag{8}$$

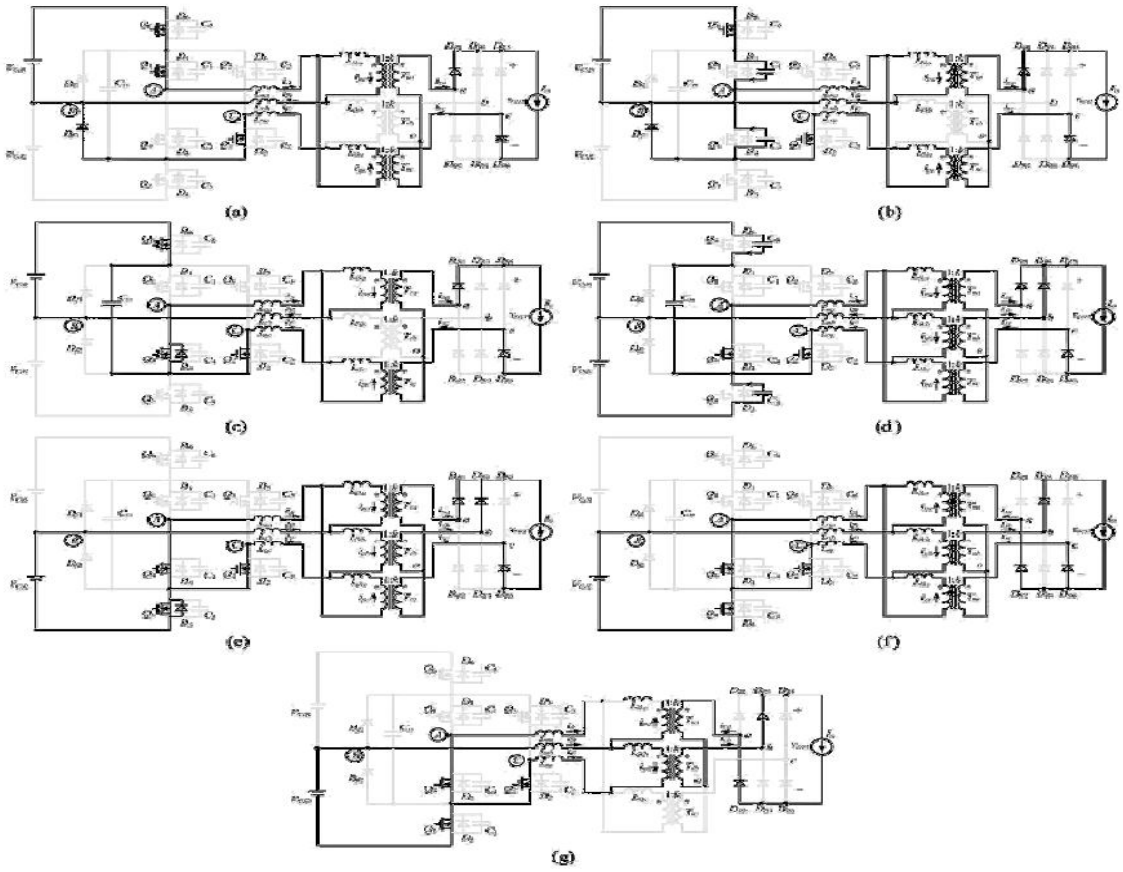


Fig. 4. Equivalent circuits under different operation stages. (a) Prior tot0.(b)[t0,t1]. (c)[t1,t2]. (d)[t2,t3]. (e)[t3,t4]. (f)[t4,t5]. (g)[t5,t6].

The modified TPTL converter has almost the same problems to closing the feedback loop as the asymmetrical half-bridge converters. The phase lag caused by the double pole–double zero of the transfer function can cause stability problems, for the phase margin is small or even null under some loads. In the practical design, the following considerations should be emphasized to achieve a better dynamic performance: 1) Combination of multilayer capacitors in parallel with electrolytic capacitors in the input capacitor design. The combination of both type of capacitor can dump the effect of the double-pole double-zero effectively. 2) A lead–lag controller should be introduced into the closed-loop design, which put both zeros of the lead–lag controller at a frequency below the double-pole frequency. Thus, the phase margin at the frequencies near the double pole–double zero effect is quite large. With the lead–lag controller, the modified converter can achieve a larger phase margin and a higher band-width than that with a single PI controller, which will be favorable to obtain a more stable steady behavior and a faster dynamic response.

Proposed Concept with 5 level converter:

The 5 level converter reduces the harmonics, when it was first used in a three-level converter in which the mid-voltage level was defined as the neutral point. The 5 level converter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level 5 level converter needs m-1 capacitors on the dc bus. A single-phase five-level converter is shown in Fig. 1.9. The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage *Vdc*, the voltage across each capacitor is *Vdc*/4, and each device voltage stress will be limited to one capacitor voltage level, *Vdc*/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward.

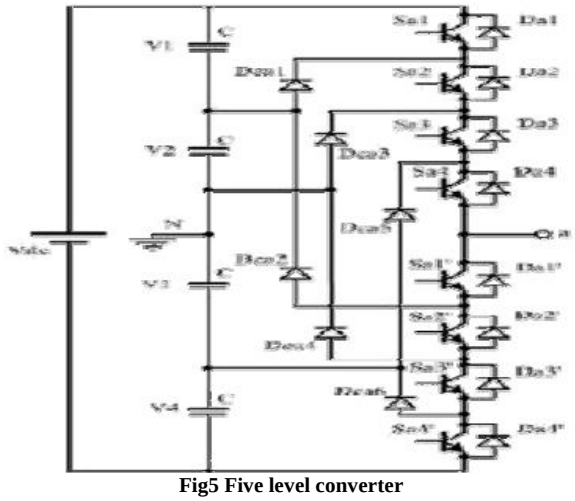
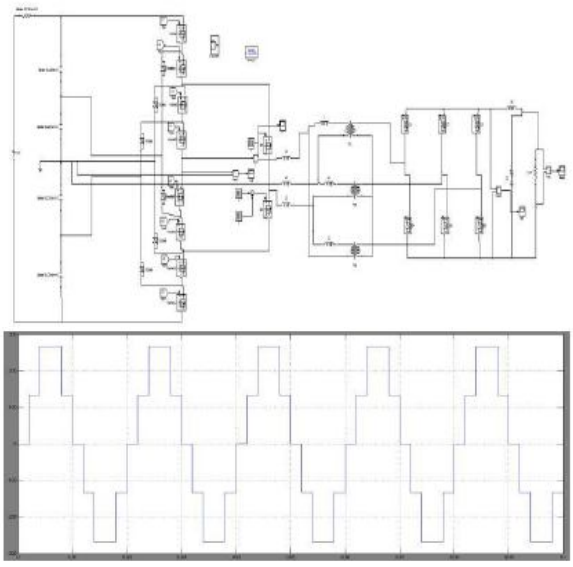


Fig5 Five level converter

To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level converter shown in Fig.5, there are five switch combinations to generate five level voltages across A and O. Table 2 shows the phase voltage level and their corresponding switch states. From Table 2, state 1 represents that the switch is on, and state 0 represents the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There exist four complimentary switch pairs in each phase, i.e., Sa1-Sa1', Sa2-Sa2', and Sa4-Sa4'.

Table II: five-level converter voltage levels and their switch st*ates*

Output V_{AO}	Switch state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a1'}$	$S_{a2'}$	$S_{a3'}$	$S_{a4'}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0.$	0	0	0	0	1	1	1	1



Simulation result for 5 level converter

CONCLUSION

A modified asymmetrical duty cycle control strategy with ZVS capability was proposed for the TPTL converter in this paper. The proposed control scheme features are- Compared with the symmetrical duty cycle control, the dominant advantages can be maintained including the lower power rating of switches and the reduced output filter requirement. The input capacitors can realize automatic and inherent voltage balancing, which ensures that all the switches sustain only one-half of the input voltage. The TPTL converter will operate in three operation modes along with the variation of duty cycle and output current, i.e., SDCM, MDCM in which, the output voltage cannot be modulated under LDCM. Three level converter has higher harmonic order so we replaced with five level converter for reduction of harmonics.

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