DESIGN AND IMPLEMENTATION OF DIFFERENT PARAMETERS OF RING OSCILLATOR USING TAIL TRANSISTOR

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Abstract— This paper represents the design and implementation of ring oscillator using microwind3.1 software in 90nm, 65nm, 25nm technology. Ring oscillator consists of an odd number of stages with feedback circuit which forms a closed loop in which output of each stage depends on the output of previous stage. The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back to the first. In this paper, three stage ring oscillator have been designed and simulated for various parameters such as phase noise, figure of merit and power consumption. Power consumption, figure of merit, phase noise have been reduced in ring oscillator.

Index Terms— Oscillator, Phase Noise, Figure of Merit, Inverter, Tail Transistor.

I. INTRODUCTION

Many electronic systems contain different types of oscillator which are used for generating the signal. Designing in CMOS technology is powerful and it gives high performance. So CMOS technology continues to raise interesting challenges. This technology squanders less power during static. So that large number of modern integrated circuits have manufactured on CMOS technology process. This paper contains Ring oscillator that are designed using Microwind3.1 software in different technologies like 90nm, 65nm and 25nm technology. The main challenge in the design of Ring oscillator is to achieve low phase noise while maintaining low power consumption as well as figure of merit. Capacitor is having poor quality factor and this directly affects on phase noise performance. Hence phase noise performance is improved by increasing the quality factor.

The relationship that power consumption of the VCO depends on transistor sizes rather than operating frequencies[1]. Ring Oscillator gives meaningful strategy for design optimization as compared to LC Oscillator[3]. It shows that the oscillator's short start-up and frequency switching transients have negligible effects on the accuracy of the TDC measurements[4]. The benchmark FOM and phase noise for PLL can be analyzed [6]. The dual mode ring oscillator operates in two different modes I) A linearization mode II) Steady state behavior which covers two different frequency bands such as 2–5 GHz and from 0.1–2 GHz[8]. Cyclic coupled ring oscillator provide several unique features over regular ring oscillators such as availability of multiple sets of phase-shifted outputs and reduced phase noise[9]. There is always need to measure or monitor circuit performance during manufacturing and at runtime[10]. Designing of high speed low power voltage control Ring Oscillator is suitable for PLL circuits[11]. The effect of frequency of oscillations, number of stages and power dissipation on the phase noise and jitter can be measured[13]. To achieve a low phase noise, fast rail to rail switching is required[14].

II. IMPORTANT PARAMETERS

1) PHASE NOISE:

The oscillator noise performance is quantitatively evaluate by interpreting a suitable signal to noise ratio. Phase Noise is a parameter that is used to determine the frequency stability of the periodic signal. It is the ratio of signal power to the noise power. If phase noise is increased then it directly affects on the performance of the system. The main feature of an oscillator is to produce similar frequency over a described period of time. Phase Noise can be calculated by

$$S_{SSB} = \frac{FKT\omega_0^2}{2P_sQ^2\Delta\omega^2} \quad (1)$$

Where,
S_{SSB}=Phase Noise of an oscillator
F= Noise Factor
K= Boltzman Constant ($1.38*10^{-23}$)
$P_{S=}$ Average Signal Power
T= Temperature
But Signal Power Can be calculated as,

$$P_S = I^2R$$

2) FIGURE OF MERIT

Figure of merit is the number which is used to distinguish the performance of the various systems. If quality factor is high then good figure of merit is achieved. Figure of merit is always expressed in dB and it can be calculated as,

$$FOM = \frac{P_SQ^2}{P_CKT} \quad (2)$$

Where,
P_C= Calculated Power

III. BASIC RING OSCILLATOR

The main purpose of an oscillator is to generate the signal which is periodic in nature. A simple three stage ring oscillator is as shown in the Fig. 1. A ring oscillator is made up of an odd number of NOT gates. The NOT gates or inverters are attached in a cascade manner and the output of the last inverter is fed back to the first. Because a single inverter computes the logical NOT of its input, it can be shown that output of a last inverters is the logical NOT of the first input.

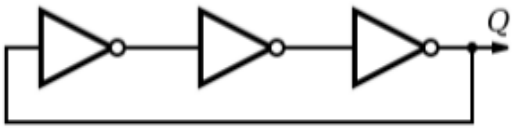

Figure 1: Three stage Ring Oscillator

IV. PROPOSED SYSTEM

A. Without Tail Transistor Topology:

Without Tail Transistor Topology for Ring Oscillator is shown in Fig. 2 . This circuit simply built from a pair of nMOS and pMOS transistors. To achieve the oscillations, ring must provide a phase shift of 2π. Frequency is directly depends on the number of stages. As increasing number of stages, frequency will decrease accordingly. Ring Oscillator is having less power consumption as well as phase noise as compared to the LC Oscillator.

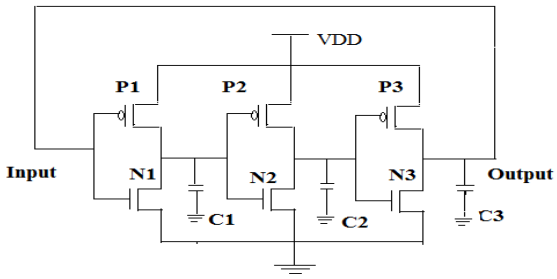

Figure 2: Without Tail Transistor Topology

B. Fixed Biased Tail Transistor Topology

Fixed Biased Tail Transistor Topology is as shown in the Fig. 3. The Tail transistor is always operate in saturation region. If amplitude grows closer to the supply voltage, the active devices will go into the triode region. This topology gives better phase noise and power consumption as compard to the Without Tail Transistor Topology.

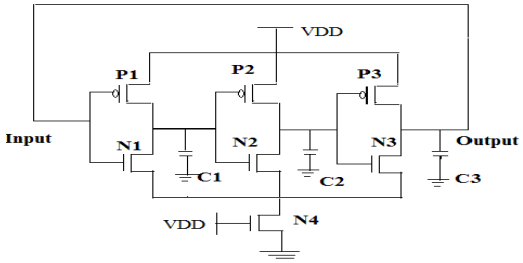

Figure : 3 Fixed Biased Tail Transistor Topology

C. Memory Reduction Tail Transistor Topology

Memory Reduction Tail Transistor Topology is as shown in Fig. 4 . This topology gives the better phase noise performance as well as figure of merit. In this topology, tail transistor operate in triode region as it shows lower flicker noise than the transistor which is operate in saturation region.

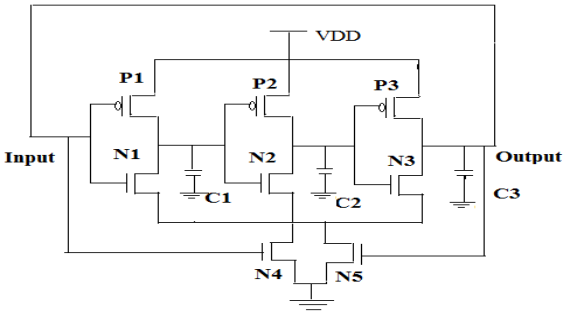

Figure 4: Memory Reduction Tail Transistor Topology

V. SIMULATIONS AND EXPERIMENTAL RESULTS

A. Without Tail Transistor Topology

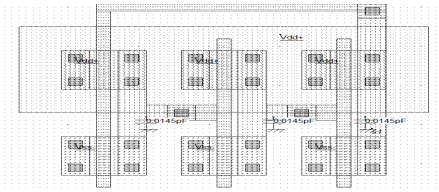

Figure 5: Layout for Without Tail Transistor Topology

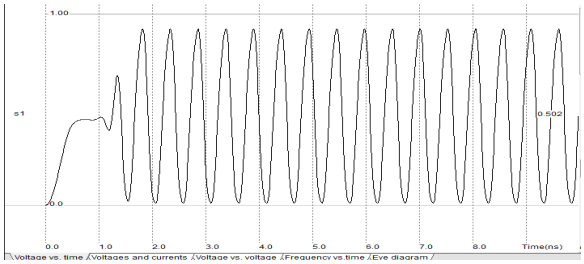

Figure 6: Output of Without Tail Transistor Topology

B. Fixed Biased Tail Transistor Topology

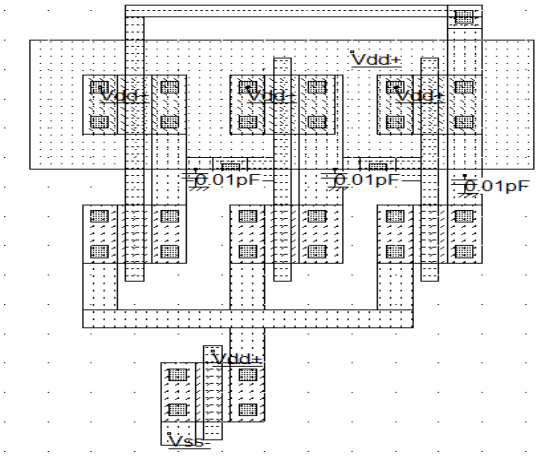

Figure 7: Layout for Fixed Biased Tail Transistor Topology

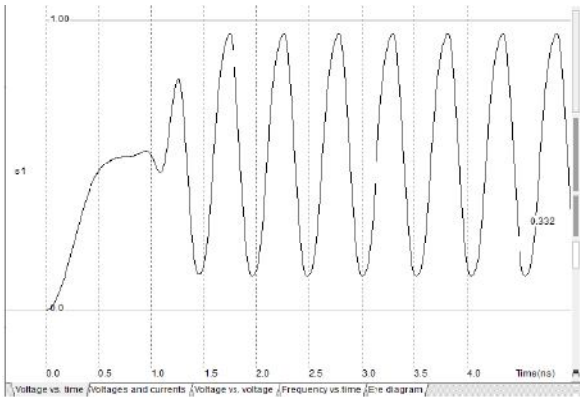

Figure 8: Output of Fixed Biased Tail Transistor Topology

C. Memory Reduction Tail Transistor Topology

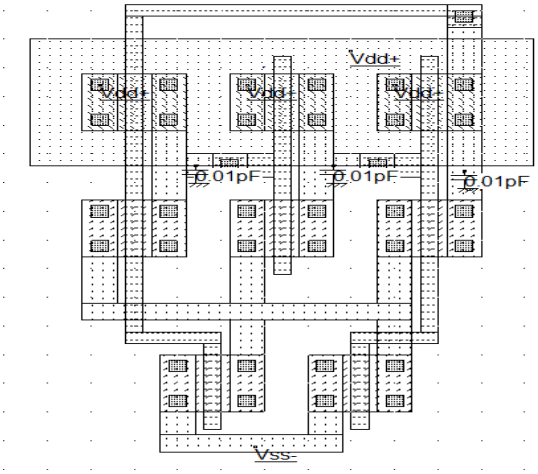

Figure 9: Layout for Memory Reduction Tail Transistor Topology

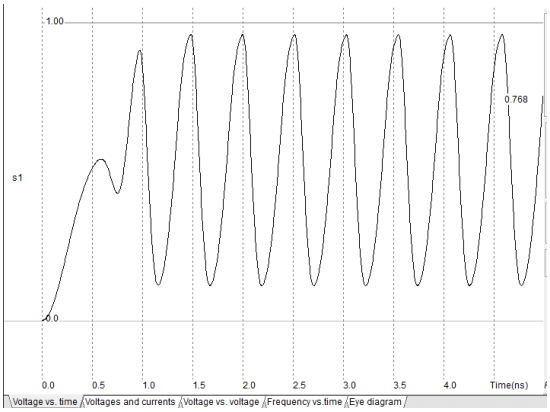

Figure 10: Output of Memory Reduction Tail Transistor Topology

CONCLUSION

The Ring Oscillator using Tail Transistor Topology has been designed and simulated by using Microwind3.1 software in 90nm, 65nm and 25nm technology. Figure of Merit, Phase noise and Power consumption are measured and reduced to increase the efficiency of oscillator. The Ring Oscillators are commonly used in clock generating signals. And also it is used during wafer testing to measure the effects of manufacturing process variations and used to measure the effects of temperature and voltage on a chip. The novel topology gives -193 dBc/Hz phase noise performance while maintaining low power consumption which is 72.71µW.

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